UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BLAISE B. FANNING
and THOMAS A. PIAZZA

Appeal No. 2006-0115
Application No. 09/823,126

ON BRIEF

Before THOMAS, KRASS, and DIXON, Administrative Patent Judges.
KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-30.

The invention pertains to a technique for cancelling a prefetch request by a processor, best illustrated by reference to representative independent claim 1, reproduced as follows:

1. An apparatus comprising:

a storage circuit coupled to a prefetcher to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to most recent access requests from a processor, the prefetcher generating an access request to a memory when requested by the processor; and

a canceler coupled to the storage circuit and the prefetcher to cancel the access request when the access request matches to at least P of the stored prefetch addresses, P being a non-zero integer, the canceler including a gating circuit to disable the access request to the memory when the access request is canceled.

The examiner relies on the following references:

Lopez-Aguado et al. (Lopez-Aguado)	5,996,061	Nov. 30, 1999
Jacobs	6,134,633	Oct. 17, 2000

Claims 1-5 and 11-15 stand rejected under 35 U.S.C. § 102(b) as anticipated by Lopez-Aguado.

Claims 6-10 and 16-30 stand rejected under 35 U.S.C. § 103 as unpatentable over Lopez-Aguado in view of Jacobs.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

A rejection for anticipation under Section 102 requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

With regard to independent claims 1 and 11, the examiner applies Lopez-Aguado as follows:

A storage circuit 150 is coupled to a prefetcher 202 to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to the most recent access requests from a processor (the examiner says there is a correspondence because most recent access requests that hit in the prefetch cache 106 cause new prefetch addresses to be generated and stored, or because the cache and prefetch cache by design store the most recently accessed programs and data, and any prefetching necessarily corresponds to those programs and data), the prefetcher generating an access request to a memory when requested by the processor (the examiner considers the processor to generally comprise all processing

elements above 202 in Figure 5, which includes an array 200 in addition to elements 110 and 112 of Figure 4; the examiner refers to column 5, lines 21-31, 40-44, and column 7, lines 18-24 and 50-59)

The examiner contends that the reference discloses a canceler coupled to the storage circuit and the prefetcher to cancel the access request when it matches to at least P of the stored prefetch addresses, P being a non-zero integer (the examiner point to column 7, line 66, to column 8, line 8, the reference recites "if the derived prefetch address is already stored within the prefetch queue 150, prefetching is terminated and the derived prefetch address is discarded"), the canceler including a gating circuit to disable the access request to the memory when the access request is canceled (the examiner indicates that a gating circuit to cancel the request is disclosed to the extent claimed, since the claimed function of "disabling when canceled" is met by the "discarding when terminating prefetching" of the reference; thus, contends the examiner, the claimed function of the gating circuit is met. Additionally, asserts the examiner, to discard a prefetch address based on the determination to terminate because an address is in the prefetch queue, a terminate or discard signal must be sent or not sent (switched) based upon a control signal (a match to an

address in the prefetch queue), which is the basic definition of a gating circuit) (see pages 3-4 of the answer).

Appellants' position is that while Lopez-Aguado discloses a method for invalidating data identified by a software compiler, with a prefetch engine (column 7, lines 18-19) and that prefetch addresses are discarded if the derived prefetch address is already stored within the prefetch queue, the reference fails to disclose a storage circuit to store prefetch addresses corresponding to most recent access requests, a canceler to cancel an access request when the access request matches to at least P of the stored prefetch address, and a gating circuit to disable the access request when the access request is canceled (brief-pages 6-7).

We have carefully reviewed the evidence of record, including the references and the arguments of appellants and the examiner and we conclude from such review that the examiner has established a prima facie case of anticipation with regard to claims 1-5 and 11-15 that have not been overcome by evidence or argument by appellants.

At pages 3-4 of the answer, the examiner has pointed out how each and every claimed element (of claims 1 and 11) is alleged to

have been met by the disclosure of Lopez-Aguado. Where specific elements are not explicitly shown, e.g., a gating circuit, the examiner explains how Lopez-Aguado is interpreted to disclose such an element. In our view, the burden had been shifted to appellants to overcome the examiner's prima facie case, if they could, by convincing rebuttal.

Appellants argue, first, that there is no gating circuit, as claimed, disclosed by Lopez-Aguado. The examiner agrees that no gating circuit is explicitly shown by the reference, but that in view of the broad functional recitation of a "gating circuit to disable the access request to the memory when the access request is canceled," the examiner finds that this recitation is met by the disclosure, at column 7, line 65 through column 8, line 5, of the reference:

> ...if the derived prefetch address is already stored within the prefetch queue 150, prefetching is terminated and the derived prefetch address is discarded. If, on the other hand, the derived prefetch address is not already in the prefetch queue 150, the derived prefetch address is provided to the EMC 108 for retrieval of a corresponding row of data from external memory.

It is the examiner's view, and we agree, that appellants show no particular structure of a specific gating circuit, the specification and drawings showing only a labeled box 350, in

Figure 3, and a description, at page 11 of the specification, that the gating circuit

> gates the access request to the memory 140. If the cancellation request is asserted, indicating that the access request for the prefetch operation is canceled, the gating circuit 350 disables the access request. Otherwise, if the cancellation request is negated, indicating that the access request is accepted, the gating circuit 350 allows the access to proceed to the memory 140.

Such description appears, to us, to be equivalent to the description, at column 7, line 65 through column 8, line 5, of Lopez-Aguado, cited supra.

Appellants argue that the examiner has not met the burden of proof necessary to establish inherency of a gating circuit in the reference. While it is true that inherency may not be established by probabilities or possibilities, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981), the examiner has shown that the claimed function of the gating circuit is taught by Lopez-Aguado, i.e., disabling an access request to a memory when the access request is canceled, and, therefore, the "gating circuit, as claimed, is taught by Lopez-Aguado. Thus, it is clear to us that whatever structure in the reference is performing the disclosed function of terminating the prefetching operation under one

condition and providing the derived prefetch address under another condition is a "gating circuit," as broadly claimed by appellants.

Appellants next argue that Lopez-Aguado does not disclose a prefetch address because it discloses a "derived" prefetch address. We agree with the examiner that the manner in which Lopez-Aguado derives a prefetch address is immaterial to the claimed subject matter. Appellants merely point out that Lopez-Aguado discloses that the derived prefetch address is the sum of a stride and an extracted physical address (column 7, lines 18-20) and assert that "the derived prefetch address is not the same as the prefetch address" (brief-page 8). However, appellants never explain why they believe this to be true, and they never distinguish their "prefetch address" from the "derived prefetch address" of the reference. It appears to us that, in its broadest sense a "derived prefetch address" is still a "prefetch address." Since appellants have convinced us of no error in the examiner's rationale, we find for the examiner.

Finally, appellants argue that Lopez-Aguado does not disclose matching with the most recent prefetch addresses. It is the examiner's position that the reference discloses this in determining if a derived prefetch address is already stored within

the prefetch queue (see column 7, line 65 through column 8, line 5) because in order to make that determination, one would need to see if the access request "matches" to at least P of the stored prefetch addresses, P being a non-zero integer. The examiner's reasoning appears valid since one is looking for a match when determining whether one address already exists somewhere else.

Appellants contend that "determining if the derived prefetch address is already in the queue is not, expressly or inherently, equivalent to matching at least P prefetch address in the queue" (brief-page 9), but appellants never state why they believe this to be the case, especially in view of the examiner's reasonable rationale. If appellants are somehow contending that the reference searches, or matches, but a single prefetch address, we note that P, being a non-zero integer, may be the integer "1." Thus, while appellants contend that the determination by Lopez-Aguado is not "equivalent to matching at least P prefetch address in the queue" (brief-page 9), appellants make no distinction between the determination of Lopez-Aguado and the matching of the instant claimed subject matter.

Moreover, appellants contend, Lopez-Aguado "does not disclose that the address in the queue represent the most recent access

requests from a processor" (brief-page 9). Again, appellants do not explain their position and, accordingly, we find it unconvincing of patentability in view of the examiner's reasonable explanation that the claims state only that "the prefetch addresses *correspond* to the most recent access requests, and such correspondence may be simply due to addresses being part of a same program or data group in the cache and prefetch cache at a certain time" (answer-page 9). The examiner continues the explanation that, "by design," caches and prefetch caches "store the programs and data that have been most recently accessed. Notwithstanding, any prefetch addresses in the queue necessarily *represent* most recent addresses, since in general prefetch addresses in the queue represent programs and data that have been most recently accessed" (answer-page 9). Appellants never offer an explanation as to why the derived prefetch addresses in the queue of Lopez-Aguado would not represent the most recent access requests from a processor.

Since we are unconvinced by any of appellants' arguments and we view the examiner as having presented a prima facie case of anticipation, we will sustain the rejection of claims 1-5 and 11-15 under 35 U.S.C. § 102(b).

Turning to the rejection of claims 6-10 and 16-30 under 35 U.S.C. § 103, the examiner applies Lopez-Aguado as above, noting that the reference lacks a teaching of a plurality of comparators to compare the prefetch address with the stored addresses, combining the comparison results, and matching of entries with a CAM. The examiner turns to Jacobs for the teaching, in a prefetching circuit, of a fully associative comparison with elements of the prefetch queue (citing Figure 2, and column 6, line 64 through column 7, line 10). The examiner asserts that "fully associative" memory "means that an input address is compared with all stored addresses simultaneously, thus requiring a plurality of comparators, combining results in order to have an indication of a match, and by definition is content addressable and thus a CAM" (answer-page 5).

The examiner contends that it would have been obvious, within the meaning of 35 U.S.C. § 103, to combine Jacobs with Lopez-Aguado because the fully associative search for the prefetch address, taught by Jacobs, is faster due to the parallel comparison with all elements in the storage. Thus, to take advantage of this faster search, the artisan would have implemented Jacob's technique in the system of Lopez-Aguado.

Appellants argue that neither Lopez-Aguado nor Jacobs discloses or suggests a gating circuit. We are unpersuaded by this argument for the reasons supra, wherein we determined that a "gating circuit" is clearly suggested in Lopez-Aguado to the same extent as claimed by appellants.

Appellants further argue that neither reference discloses a plurality of comparators to compare the current prefetch address with each of the stored prefetch addresses, However, the examiner has explained, reasonably, in our view, that Jacobs "fully associative" memory compares an input address with all stored addresses simultaneously, requiring a plurality of comparators, and appellants have offered nothing to convince us of any error in the examiner's reasoning.

Appellants further explain that there is no motivation to combine the references. Again, we disagree in the face of the examiner's thoughtful reasoning as to why the artisan would have been led to increase the speed of the search for a prefetch address in memory in Lopez-Aguado from the teachings of Jacobs. Appellants never explain what, if anything, is wrong with the examiner's reasoning.

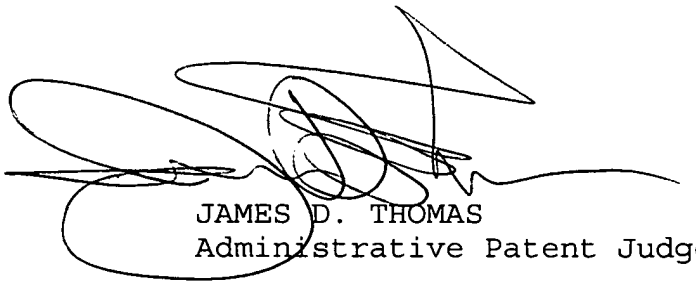
Appellants also contend that Jacobs "merely discloses using a fully associative prefetch memory when comparing the addresses of cache access operations, not comparing a current prefetch access request with each of the stored prefetch address" (brief-page 10).

However, the examiner explains that "the cache access operations described by Jacobs include the prefetch operations...Therefore, the teaching of plurality of comparators for comparing an incoming address which may be a prefetch address to a queue of prefetch addresses may be applied to the prefetch queue of Lopez-Aguado..." (answer-page 10). It does seem reasonable that cache access operations would include prefetch operations, viz., a current prefetch access request, and we note that appellants do not dispute this allegation by the examiner that cache access operations include prefetch operations. Accordingly, since appellants have not convinced us of any error on the examiner's part, we will sustain the rejection of claims 6-10 and 16-30 under 35 U.S.C. § 103.

The examiner's decision rejecting claims 1-5 and 11-15 under 35 U.S.C. § 102(b) and rejecting claims 6-10 and 16-30 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED



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